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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,037	06/08/2005	Tadahiko Hirai	03500.017994	1450
5514 7590 04/10/2008 FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112				
EXAMINER TRAIL, ALLYSON NIEL				
ART UNIT		PAPER NUMBER		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

## Application No.

10/538,037

## Applicant(s)

HIRAI, TADAHIKO

## Examiner

ALLYSON N. TRAIL

## Art Unit

2876

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are REJECTED.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date 8/06, 10/06
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_

**DETAILED ACTION**

***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

2. The Information Disclosure Statements filed on August 10, 2006 and October 10, 2006 have been considered. An initialed copy of the Form 1449 is enclosed herewith.

***Claim Objections***

3. Claims 4 and 5 are objected to because of the following informalities:  
Re claims 4 and 5, line 3: replace "its" with --the resistor's element's--.  
Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:  

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 7 and 8 recite that the integrated circuit contain a clock frequency and a power supply voltage respectively which is different from that in a specification. It is unclear what the phrase "different from that in a specification" is referring to. Please clarify.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 6-8, 10, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Gercekci et al (4,841,133), hereinafter Gercekci. Additionally, as is discussed above, claims 7 and 8 are rejected under 112, second paragraph as being indefinite. However the claims are being examined with the interpretation of that the integrated circuit contains a clock frequency (claim 7) and a power supply voltage (claim 8).

With respect to claim 1, Gercekci discloses in the abstract an unauthorized access prevention method for an integrated circuit (also referred to as a "smart card", i.e., integrated circuit – regarding claims 10 and 15-17) including a plurality of resistor elements (fuse 28) capable of selecting between a high and low impedance state irreversibly in an interface portion within the integrated circuit. Furthermore Gercekci discloses that when a signal (externally-applied code) is inconsistent with verification information (preprogrammed transport code) and standard that is present in the integrated circuit is received at least once, the impedance state of the resistor element (fuse) is changed from an initial state to stop a part or all of accesses to the integrated circuit irreversibly.

Specifically as is taught in the abstract, the resistor element is "blown" when two codes, i.e., signals (preprogrammed transport code and an externally-applied code) do not match. It is understood that when a fuse is blown it has a relatively high impedance compared to the fuse having an unblown state.

It is further disclosed in column 1, lines 37-39 that an object of the present invention is to provide an increased level of security against the theft of un-initialized cards.

With respect to claim 6, Gercekci discloses that the verification information that is preset in the integrated circuit is a keyword/logic. Specifically, as is discussed above with regards to claim 1, the preset verification information is preprogrammed transport code. Clearly the code consists of logic and/or a keyword since it is stored in memory and compared to an externally entered code.

With respect to claims 7 and 8, Gercekci discloses in column 3, lines 1-5 that, "The control circuitry has three supply inputs - a programming voltage input 12, a supply voltage input 14 and a reference voltage input 16. It also has three ports - a data input/output port 18, a clock input 20 and a reset input 22."

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 2, 9, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gercekci in view of Dalton et al (2003/0080393), hereinafter Dalton.

Gercekci's teachings are discussed above including the limitation of claims 11 and 18, that the unauthorized access prevention method is applied to an IC card. Gercekci however fails to specifically teach the resistor element containing an organic conductor.

With respect to claim 2, Dalton discloses in paragraph 0001, that the present invention relates generally to integrated circuit devices and, more particularly, to an encapsulated, energy-dissipative fuse for use with integrated circuit devices. Paragraph 0011 further a fuse structure (resistor element) wherein an organic material is encapsulated beneath a thin, conductive layer, thereby forming a fuse structure. Paragraph 0021 details an alternative structure wherein the organic material (such as Ormecon) is itself the conductive layer.

With regards to claim 9, Dalton teaches in paragraph 0002 discloses that the invention relates to semiconductor integrated circuits. It is further disclosed in Dalton's claim 18 that the semiconductor integrated circuit comprises electrically conductive organic material.

Lastly, Dalton explains in paragraph 0005 that using the described fuse, allows the blowing of the fuse with lower applied energy while still sufficiently ablating so as not to result in short circuiting of other components.

In view of Dalton's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made use the fuse taught by Dalton as the fuse used to prevent unauthorized access to an integrated circuit taught by Gercekci. Gercekci simply teaching using a fuse to deactivate the integrated circuit,

however the specific fuse that is used is not disclosed. Dalton discloses that the fuse structure, which includes an organic conductor, is often used in integrated circuit devices and furthermore discloses that such a structure allows the blowing of the fuse with lower applied energy while still sufficiently ablating so as not to result in short circuiting of other components. Therefore in view of Dalton's teachings one would be motivated to use such a fuse so that the desired fuse is blown while maintaining the structure of the remaining circuit.

10. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gercekci in view of Cheng et al (2003/0060009), hereinafter Cheng.

Gercekci's teachings are discussed above including the limitation of claim 12, that the unauthorized access prevention method is applied to an IC card. Gercekci however fails to specifically teach the resistor element being formed of a capacitor.

With respect to claim 3, Cheng illustrates in figures 1A-1H a metal capacitor and fuse structure formed. Paragraph 0002 discloses the advantage of fuses being formed with metal-insulator-metal capacitors, wherein the advantage is that such capacitors used in integrated structures possess the ability to precisely control their capacitance based on dimensional control.

In view of Chen's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made use the fuse, which is formed with a capacitor taught by Chen as the fuse used to prevent unauthorized access to an integrated circuit taught by Gercekci. Gercekci simply teaching using a fuse to deactivate the integrated circuit, however the specific fuse that is used is not disclosed.

Chen discloses that the fuse structure, which includes a metal capacitor is often used in integrated circuit in order to precisely control the capacitance in the integrated circuit. Therefore in view of Chen's teachings one would be motivated to use such a fuse so that the capacitance of the integrated circuit can be precisely controlled. Furthermore forming the capacitor with the fuse allows for less parts.

11. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gercekci in view of Kurth et al (7,218,547).

Gercekci's teachings are discussed above including the limitation of claim 13, that the unauthorized access prevention method is applied to an IC card. Although Gercekci teaches securing the card by changing the impedance of the resistor element the specific method of applying a higher voltage to the resistor element is not disclosed.

With respect to claim 4, Kurth however discloses in column 2, lines 55-64, that the resistor element presents a high impedance between the conductive plates before being "blown" or programmed, and a relatively low impedance between the conductive plates after being programmed. To program the resistor element, a programming voltage of a sufficient magnitude is applied across the conductive plates causing a "breakdown" of the dielectric layer, which results in the dielectric layer having relatively low impedance. Kurth further discloses that resistor elements can be used in a variety of applications, including selectively enabling or disabling components on a semiconductor integrated circuit.



In view of Kurth's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to apply a higher voltage to the resistor element in order to change its impedance as is taught by Kurth, to the unauthorized access prevention method taught by Gercekci. Gercekci teaches preventing the use of a smart card by comparing an entered signal to a present signal and securing the card if the signals do not match. As is recited above, although Gercekci teaches securing the card by changing the impedance of the resistor element, the specific method of achieving the change of impedance is not disclosed. Kurth however specifically teaches achieving a change of impedance for the purpose of disabling components in an integrated circuit. Therefore one would be motivated to apply a higher than normal voltage to the resistor element since as is discussed by Kurth, doing such will result in changing the impedance of the element and in turn will disable certain integrated circuit components and result in securing the integrated circuit.

12. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gercekci in view of Khoury (2003/0011379).

Gercekci's teachings are discussed above including the limitation of claim 14, that the unauthorized access prevention method is applied to an IC card. Although Gercekci teaches securing the card by changing the impedance of the resistor element the specific method of applying a larger current to the resistor element is not disclosed.

With respect to claim 5, Khoury however discloses in paragraph 0002 using fuse or anti-fuse fusible links (resistor elements) wherein fuse links are opened by blowing

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the fuse by applying a writing current. It is further disclosed that once a fuse link is blown the impedance of the link is much higher than that of an unblown fuse.

Paragraph 0025 refers to the action of applying current to blow a fuse as "Fuse-Current-Switch".

In view of Khoury's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to apply a large current to the resistor element (fuse) in order to change its impedance as is taught by Khour, to the unauthorized access prevention method taught by Gercekci. Gercekci teaches preventing the use of a smart card by comparing an entered signal to a present signal and securing the card if the signals do not match. As is recited above, although Gercekci teaches securing the card by changing the impedance of the resistor element, the specific method of achieving the change of impedance is not disclosed. Khoury however specifically teaches achieving a change of impedance (blowing a fuse) by applying current to the fuse. Therefore one would be motivated to apply a larger than normal current to the resistor element since as is discussed by Khoury, doing such will result in blowing the fuse and moreover disabling the circuit. Furthermore one would be motivated to use a Fuse-Current-Switch as they are commonly used and therefore is widely available and low in cost.

### ***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Clark (6,895,509), Lu (2004/0068656), Biagi et al (2007/0025038), and Tour et al (2005/0101063).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Allyson N. Trail* whose telephone number is (571) 272-2406. The examiner can normally be reached between the hours of 7:30AM to 4:00PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee, can be reached on (571) 272-2398. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [allyson.trail@uspto.gov].

*All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.*

/Allyson N Trail/

Allyson N. Trail  
Patent Examiner  
Art Unit 2876

March 27, 2008